Hall Ticket Number:

Code No. : 13459 S C

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) III-Semester Supplementary Examinations, August-2023

Digital System Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10× 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	State and Prove Absorption Law and Redundancy Law in Boolean Algebra.	2	1	1	1
2.	Express the Binary number (110101) in Gray code and Hexa Decimal Number.	2	2	1	2
3.	What is a multiplexer? What is the function of a Multiplexer's select input?	2	1	2	1
4.	Draw the Logic Diagram of a 4x2 Encoder using Basic Gates.	2	2	2	1
5.	List the applications of Finite State Machines.	2	1	3	1
6.	Differentiate between Combinational and Sequential Circuits.	2	1	3	1
7.	Identify the keywords used for Data Flow model. Which of them is essential?	2	1	4	1
8.	Write Verilog HDL code for 4X1 Mux using Gate Level Modeling.	2	1	4	1
9.	Define the Logic Synthesis.	2	1	5	1
10.	What is the difference between always and initial statements?	2	1	5	1
	Part-B (5×8 = 40 Marks)				
11. a)	For the Boolean function F = xyz + x'y + xyz' obtain the truth table.	4	3	1	2
b)	Obtain the minimal sum of products expression for the following Boolean function using K-Map method. $f(A,B,C,D)=\sum m(1,4,7,8,9,11,13,14)+\sum d(0,3,5)$	4	3	1	2
12. a)	What is a combinational logic circuit? Implement a Full adder using two half adders and one OR gate.	4	3	2	2
b)	Design a 4x1 Multiplexer using 2X1 Multiplexer.	4	3	2	2
13. a)	Explain the Design steps of converting a D Flip Flop to T Flip Flop.	4	2	3	3
b)	A synchronous sequential circuit is required to divide the input clock frequency by 20. Design the circuit using D Flip Flops.	4	4	3	2

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	,uss the Design of 1 Bit Comparator with suitable Verilog code in Gate vel Modeling.	4	2	4	3
b)	Explain any two Compiler Directives in Verilog HDL.	4	2	4	1
15. a)	Identify the difference between Blocking and Non-Blocking Assignment statements and give example to each of them.	4	4	5	1
b)	Draw the Block Diagram of FPGA and explain them.	4	2	5	1
16. a)	Explain the classification of Binary Codes.	4	2	1	2
b)	Implement the function f (A, B, C) = $\sum$m (0, 2, 1, 4, 7) using 8X1 Multiplexer.	4	4	2	3
17.	Answer any ***two*** of the following:				
a)	Describe the operation of Clock Generator.	4	2	3	1
b)	Write a Test Bench Program for a 8X3 Priority Encoder.	4	3	4	1
c)	Distinguish between Tasks and Functions in Verilog.	4	2	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO; Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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